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46069 7590 03/23/2011 F. CHAU & ASSOCIATES, LLC Frank Chau 130 WOODBURY ROAD WOODBURY, NY 11797			EXAMINER WEST, JEFFREY R	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AZEEZ BHAVNAGARWALA, DAVID J. FRANK, and
STEPHEN V. KOSONOCKY

Appeal 2009-013371
Application 10/643,193
Technology Center 2800

Before ALLEN R. MacDONALD, ELENi MANTIS MERCADER, and
BRADLEY W. BAUMEISTER, *Administrative Patent Judges*.

MacDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL¹

¹ The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the “MAIL DATE” (paper delivery mode) or the “NOTIFICATION DATE” (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF CASE

Introduction

Appellants appeal under 35 U.S.C. § 134 from a final rejection of claims 1, 3-13, 15, 16, 18, 19, 26, 27, 29, 32-36, and 38. Claims 2, 14, 20-25, 28, 30, and 31 have been canceled. Claims 17 and 37 have been objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. We have jurisdiction under 35 U.S.C. § 6(b).

Exemplary Claim

Exemplary independent claim 1 under appeal reads as follows:

1. A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{out} as a function of an input DC voltage V_{in} , wherein V_{in} is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein V_{out} is obtained at a common node connection of the first and second semiconductor transistor devices, and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

Examiner's Rejections²

1. The Examiner rejected claims 1, 3, 5-10, 12, 26, 27, 29, and 32 under 35 U.S.C. § 103(a) over the combination of Cranford (US 6,275,094 B1) and Conti, *Test structure for mismatch characterization of MOS transistors in subthreshold regime*, PROC. IEEE 1997 INT. CONFERENCE ON MICROELECTRONIC TEST STRUCTURES, Vol. 10, pp. 173-78 (March 1997) (hereinafter, "Conti").

2. The Examiner rejected claim 4 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Cranford, Conti, and Haruyama (US 6,731,916 B1).

3. The Examiner rejected claims 13 and 33 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Cranford, Conti, and Zhang (US 5,999,043).

4. The Examiner rejected claims 11 and 34 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Cranford, Conti, Zhang, and Zhou (US 6,819,183 B1).

5. The Examiner rejected claims 15, 16, 35, and 36 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Cranford, Conti, and Yoshizawa (US 4,851,768).

² Separate patentability is not argued for dependent claims 3-9, 11-13, 15, 16, 18, 19, 29, 32, 34-36, and 38 rejected under 103(a). Rather, Appellants merely reiterate the arguments presented for the patentability of claims 1, 10, 26, and 27. *See* App. Br. 17-18; Reply Br. 18-19. Hence, our discussion is limited to Appellants' arguments as to claims 1, 10, 26, and 27.

6. The Examiner rejected claim 18 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Cranford, Conti, and Lovett (US 6,181,621 B1).

7. The Examiner rejected claims 19 and 38 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Cranford, Conti, and Ueda (US 6,798,278 B2).

Appellants' Contentions

1. Appellants contend that the Examiner erred in rejecting claims 1, 10, 26, and 27 under § 103 for numerous reasons, including that (1) the Examiner employed impermissible hindsight, (2) Cranford fails to teach obtaining and using DC voltage characteristic data to determine device mismatch, and instead teaches using Fast Fourier Transform (FFT) analysis of AC in/out signals to determine harmonic differences of sinusoidal in/out voltages to correlate these differences to device offset, and (3) Conti teaches away from the claimed invention because Conti measures DC current characteristic data and not DC voltage characteristic data (App. Br. 12-17).

2. Appellants also contend that the Examiner erred in rejecting claims 1, 3, 5-10, 12, 26, 27, 29, and 32 because Cranford's Figures 7 and 8 and accompanying text (*see* col. 7, l. 57 to col. 8, l. 12) disclose a DC component of the output that is a zero frequency component of an AC signal (Reply Br. 17). Thus, Appellants assert that the DC component is "simply a constant displacement from equilibrium at zero frequency," which means that "the DC component of Cranford cannot be interpreted as comprising 'an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN} ' essentially as claimed" (Reply Br. 17 (emphases in original)). In other words, Appellants assert that Figure 8 of Cranford does not disclose finding a DC

output voltage as a function of a DC input voltage (App. Br. 15). Appellants contend that Cranford's DC component (i) is a zero frequency component that is "essentially removed" as a result of the FFT analysis (Reply Br. 17), and (ii) is a constant and does not indicate a threshold mismatch (Reply Br. 17-18).

Issues on Appeal

1. Did the Examiner err in rejecting claims 1, 3-13, 15, 16, 18, 19, 26, 27, 29, 32-36, and 38 as being unpatentable because Cranford does not teach or suggest obtaining and using "DC voltage characteristic data" to determine device mismatch, as required by claims 1, 10, 26, and 27, and instead operates on AC data?

2. Did the Examiner err in rejecting claims 1, 3-13, 15, 16, 18, 19, 26, 27, 29, 32-36, and 38 as being unpatentable under § 103 because Conti measures DC *current* characteristic data, and therefore teaches away from Appellants' claimed invention?

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' arguments in the Appeal Brief and Reply Brief that the Examiner has erred.

We disagree with Appellants' conclusion. We adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to Appellants' Appeal Brief. We concur with the conclusion reached by the Examiner.

First Issue

We agree with the Examiner (Ans. 16) that Appellants admit Cranford teaches “a method for dynamically generating a *voltage* to correct threshold mismatch between transistor devices in a differential amplifier to thereby correct for manufacturing offset (See Abstract; and Col. 7, lines 20-23)” (App. Br. 14 (emphasis added)). We also agree with the Examiner’s interpretation of the term ““DC voltage characteristic data”” as encompassing “any data that pertains to DC voltage,” and not just isolated DC data (Ans. 17).

Accordingly, we agree with the Examiner’s findings and analysis in the Answer (Ans. 20-21), that Cranford’s measured input/output signals (*see* Fig. 6 and col. 7, ll. 44-47; inputs 112 and 114, outputs 116 and 120) contain “DC voltage characteristic data” inasmuch as this phrase is defined in the claims on appeal. Because Cranford determines mismatch between two devices and corrects for voltage offset using a *voltage* supply 158 (*see also* processor 151 and voltage level table 156 used to determine the offset voltage to be applied; Fig. 5 and col. 7, ll. 20-36), Cranford teaches or suggests DC voltage characteristic data such as an output DC voltage which is a function of an input DC voltage as set forth in claims 1, 10, 26, and 27.

In other words, we agree with the Examiner that in order to determine DC voltage offset used in Cranford’s Figure 5 (at 158) to correct for mismatch, “the DC voltage offset must first be measured” (Ans. 21). Thus, Cranford’s disclosure teaches or suggests obtaining and using an output DC voltage in relation to an input DC voltage to determine device mismatch.

Second Issue

Appellants' contention that Conti measures DC *current* characteristic data, and therefore teaches away from Appellants' claimed invention is unconvincing. As pointed out by the Examiner, Conti is not relied upon for teaching measuring drain current, but for measuring characteristics of transistor device pairs operating in a subthreshold region (Ans. 23-25). Conti is related to the problem addressed in Appellants claims and by Cranford, that of the analysis and determination of device mismatch by providing an estimate of threshold mismatch using test circuits.

CONCLUSIONS

(1) The Examiner has not erred in rejecting claims 1, 3-13, 15, 16, 18, 19, 26, 27, 29, 32-36, and 38.

(2) Claims 1, 3-13, 15, 16, 18, 19, 26, 27, 29, 32-36, and 38 are not patentable.

DECISION

The Examiner's rejections are affirmed.

Appeal 2009-013371
Application 10/643,193

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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